

[illegible][illegible]

[illegible]

Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 10C with a VSub contact. A stack of layers 1A, 1B, and 1C is shown. Layer 1A contains regions 7A and 7B, and layer 1B contains regions 8 and 11. A VBG contact is shown at the bottom. Other labels include 1, 2, 3, 4, 9, and 10C.

FIG. 5

FIG 5(A)

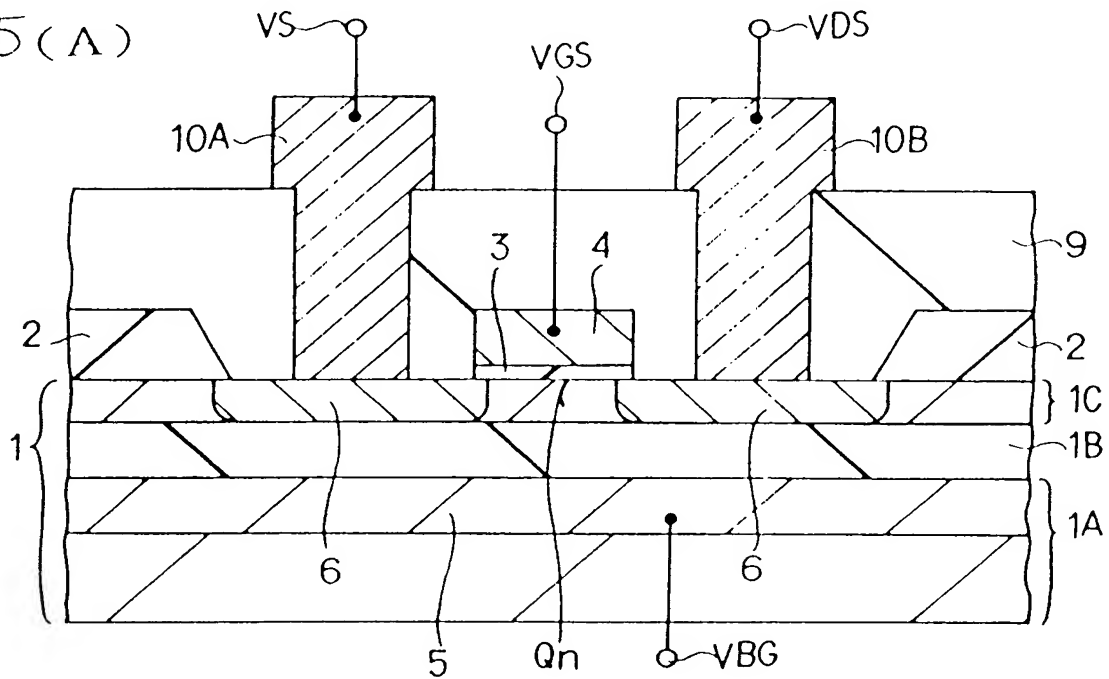


FIG 5(B)

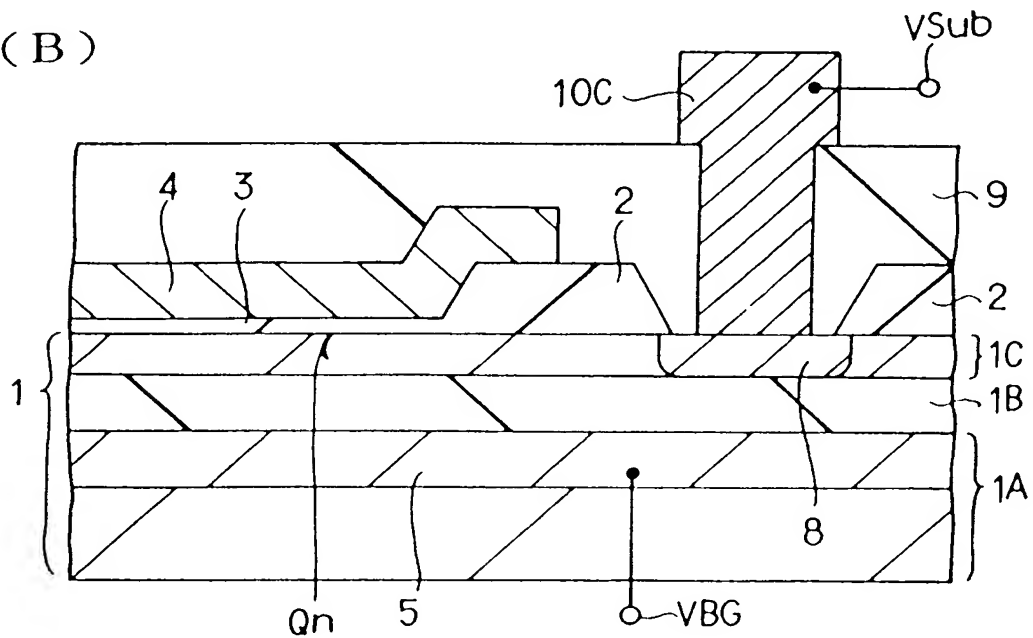


FIG. 10

FIG. 10(A)

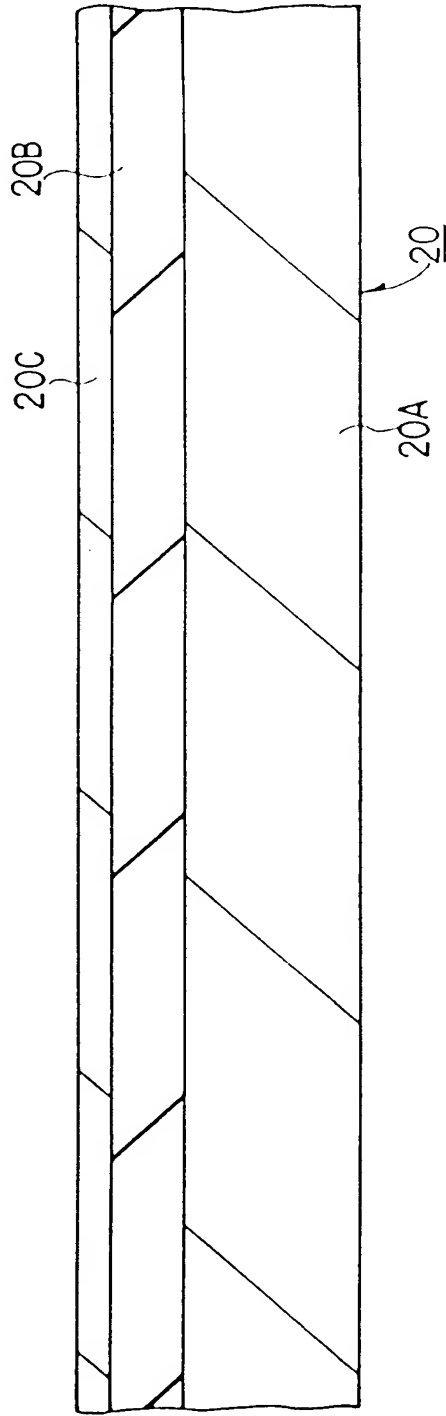


FIG. 10(B)

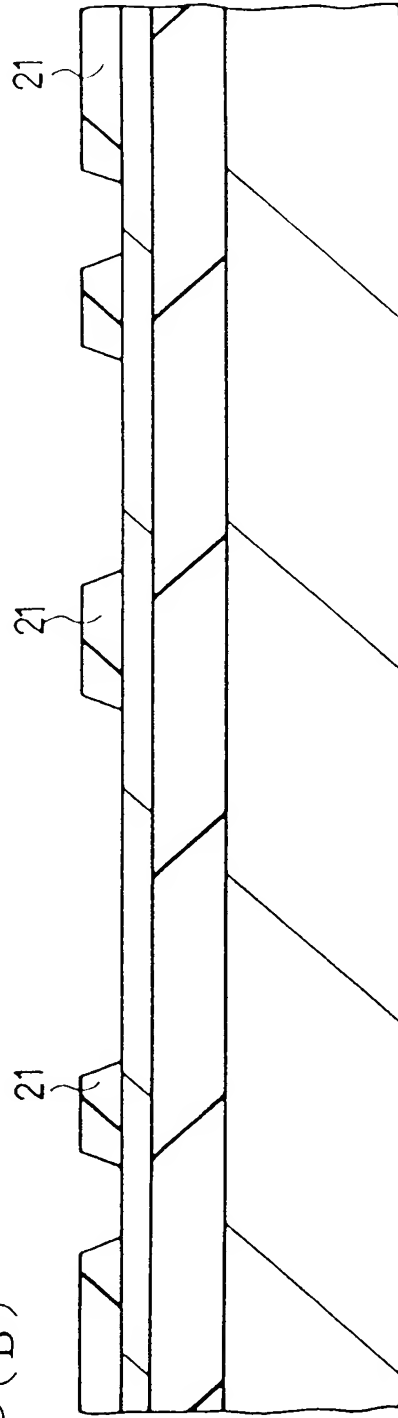


FIG. 11

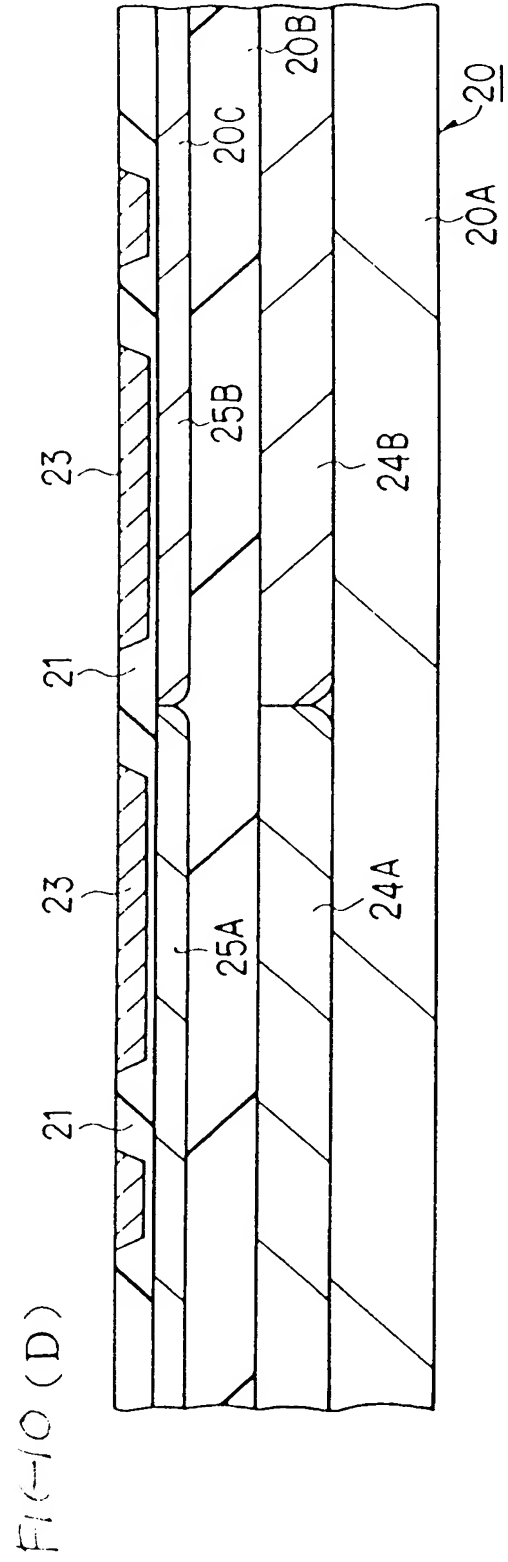
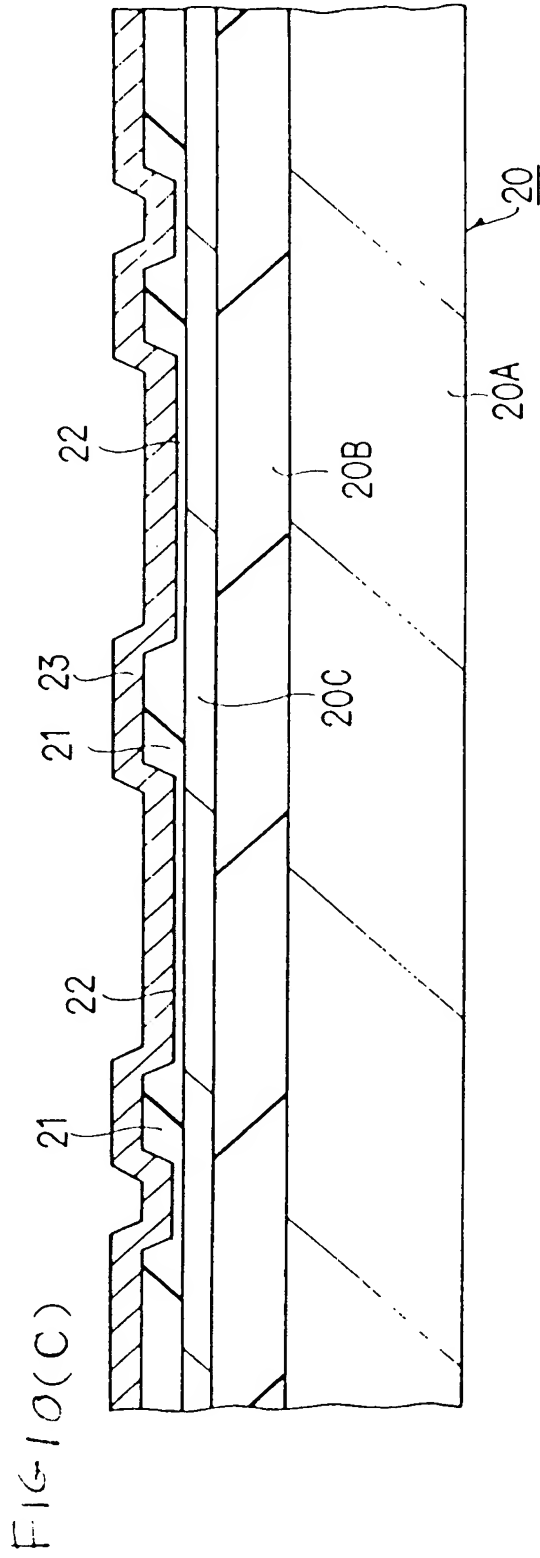




FIG. 11  
FIG. 13

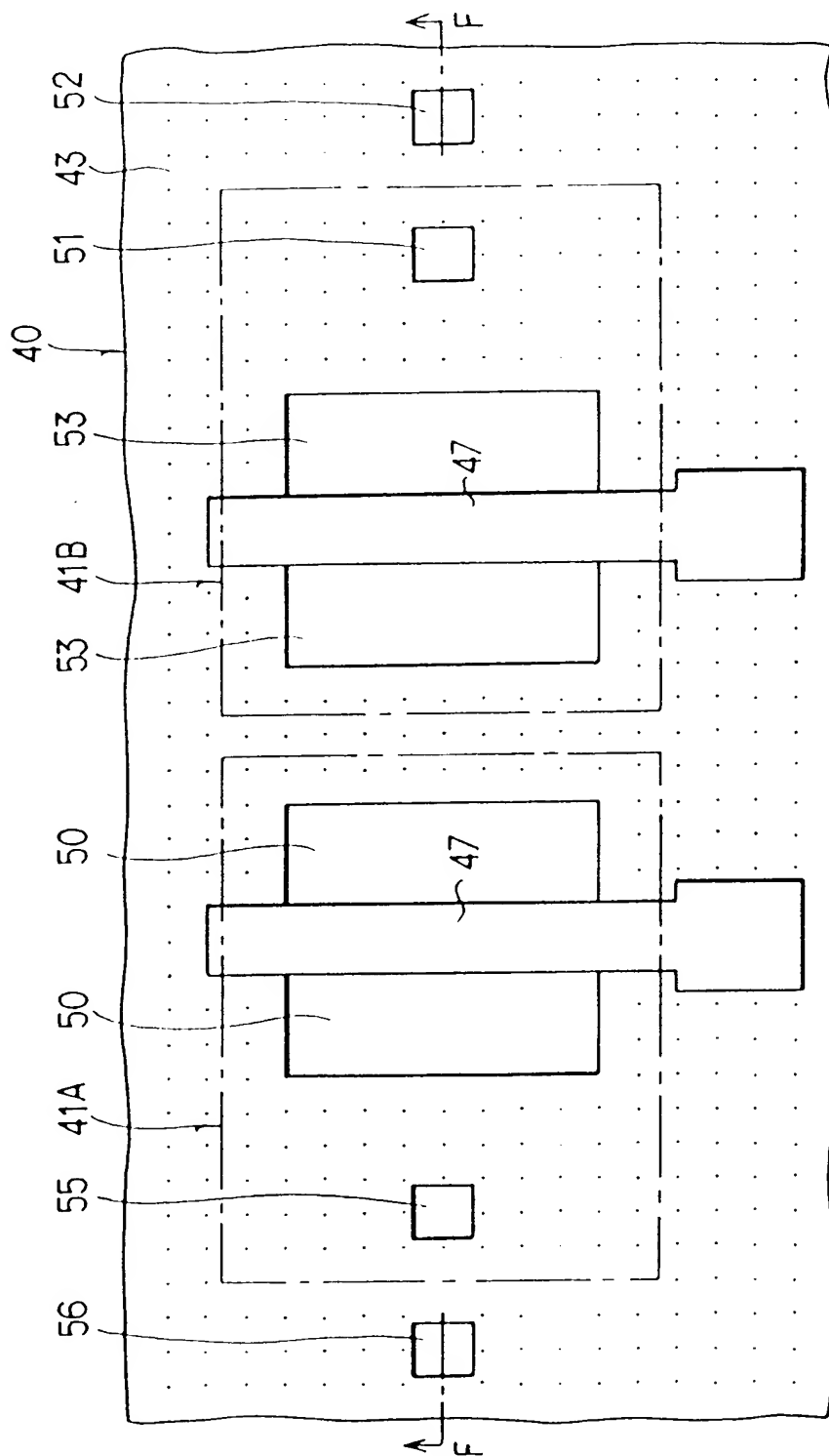


FIG. 12.  
FIG. 14.

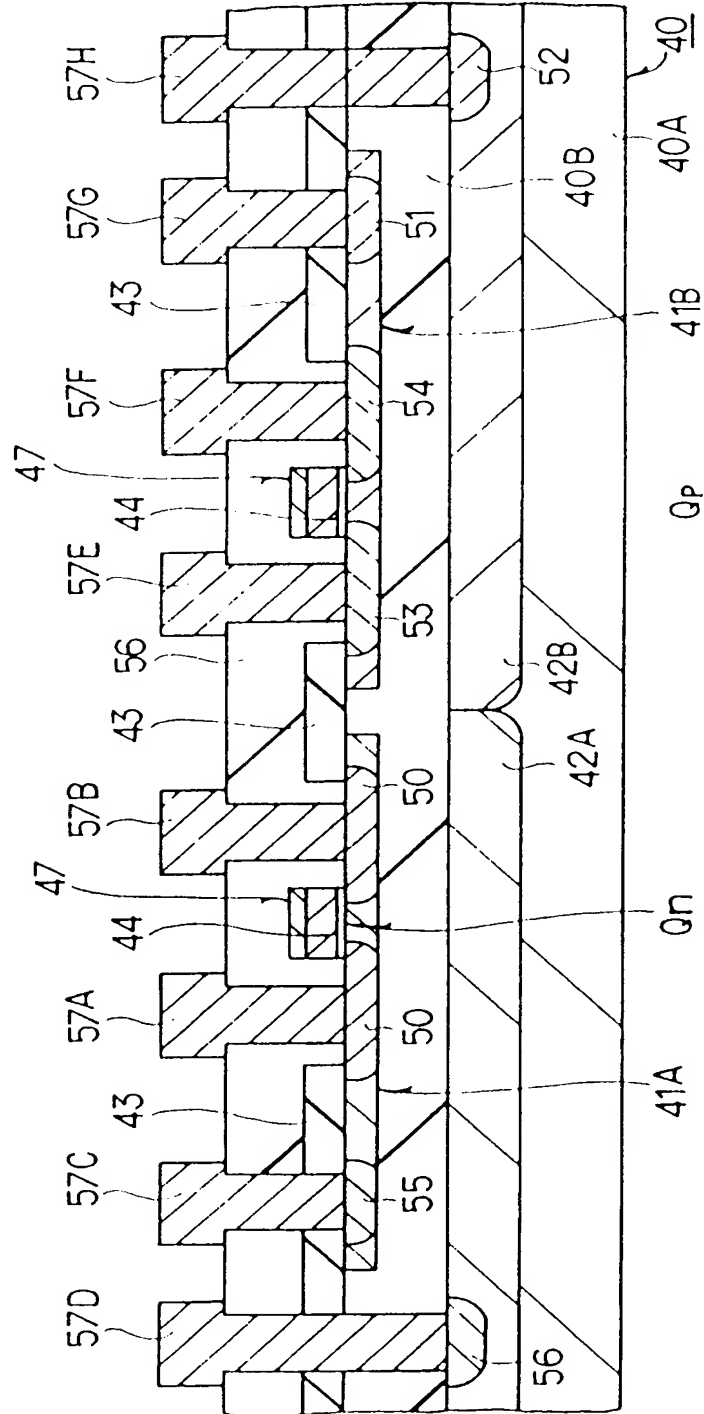




FIG. 15

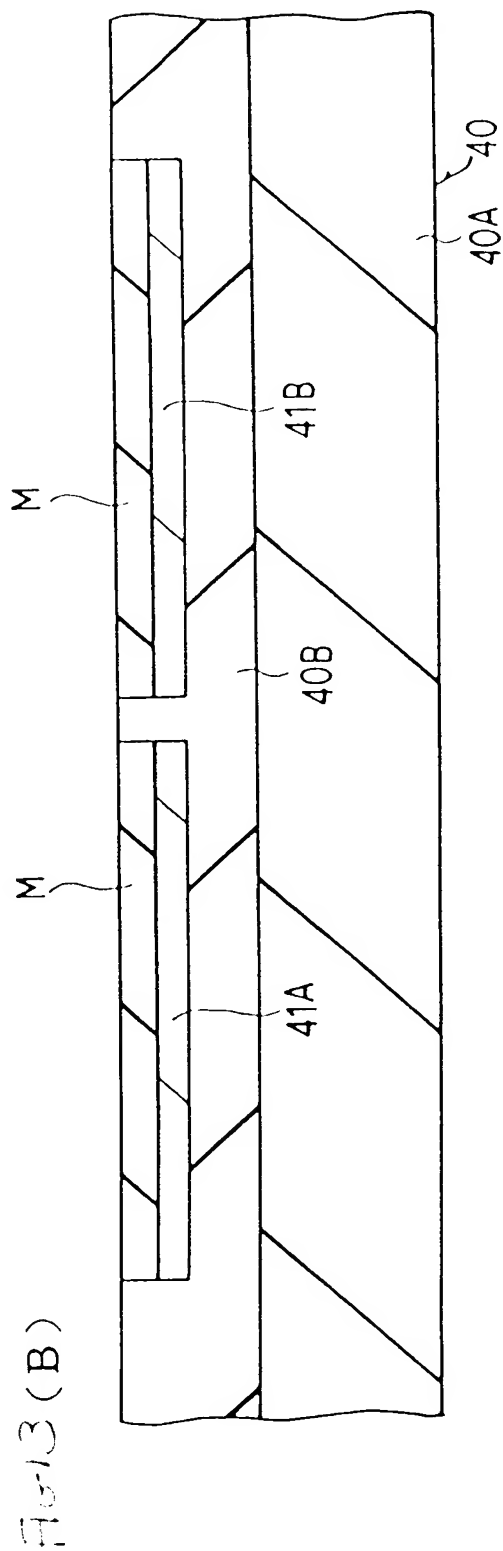
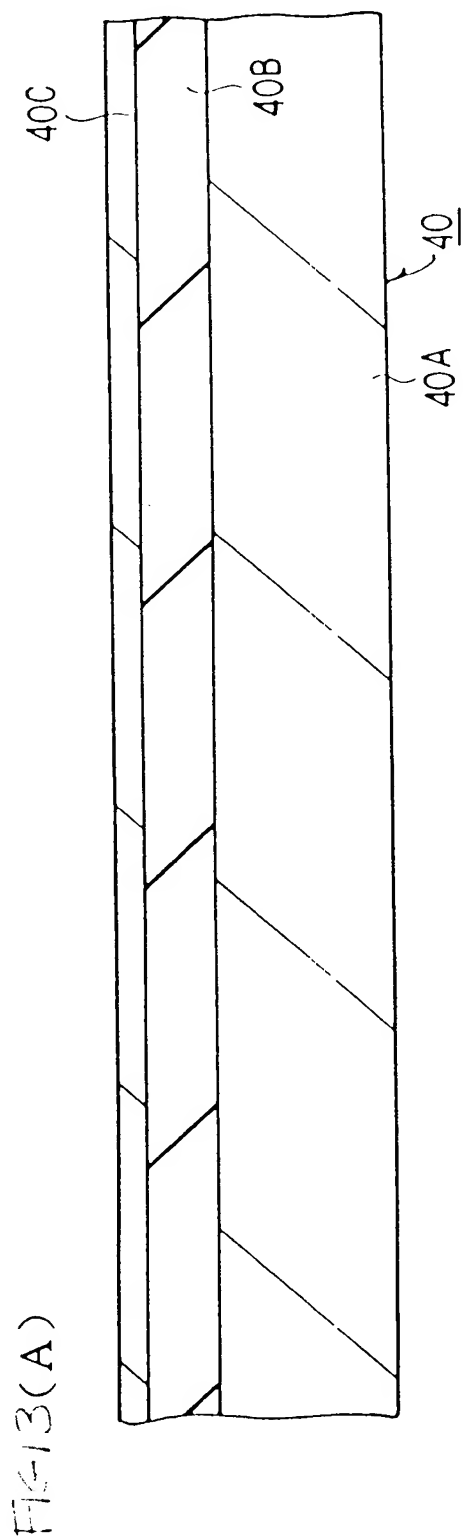


FIG. 10

FIG 13(C)

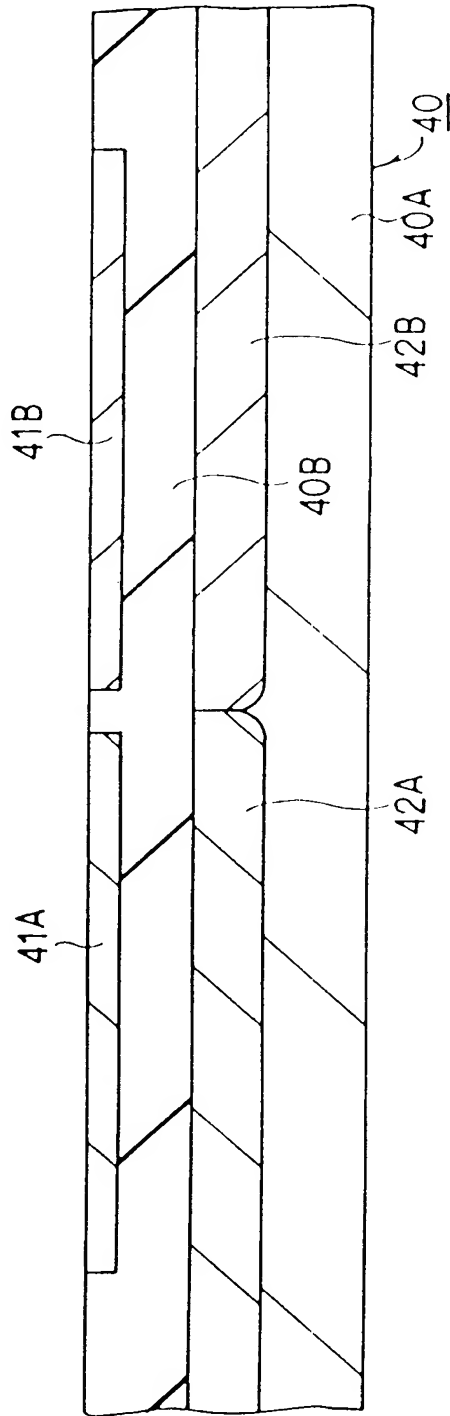


FIG 13(D)

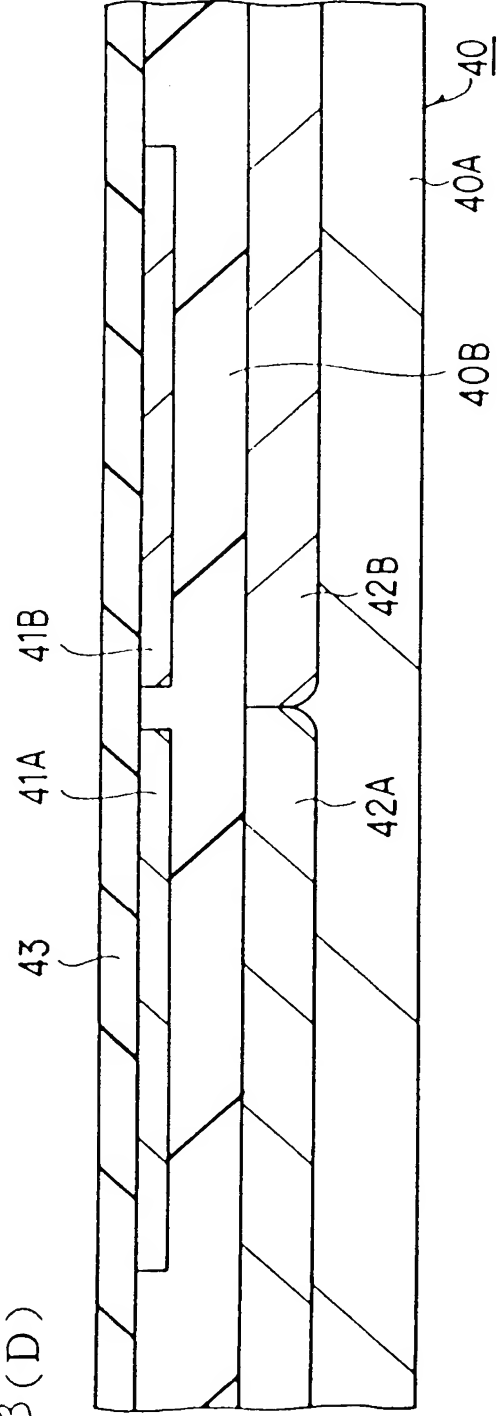


FIG. 17-

FIG. 13(E)

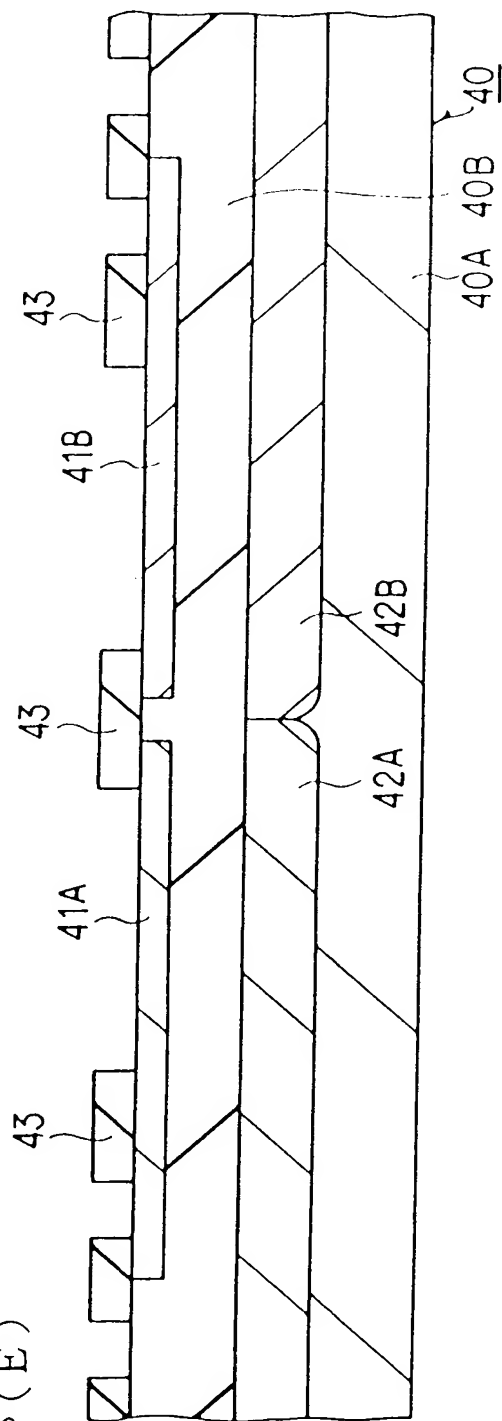


FIG. 13(F)

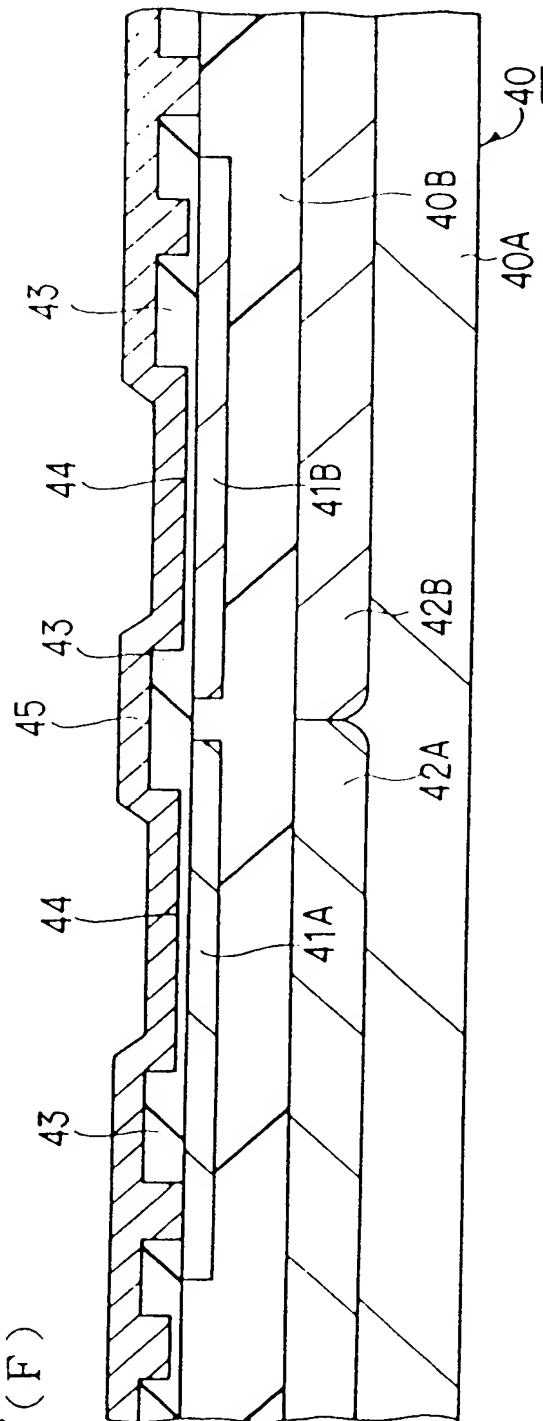


FIG. 18-

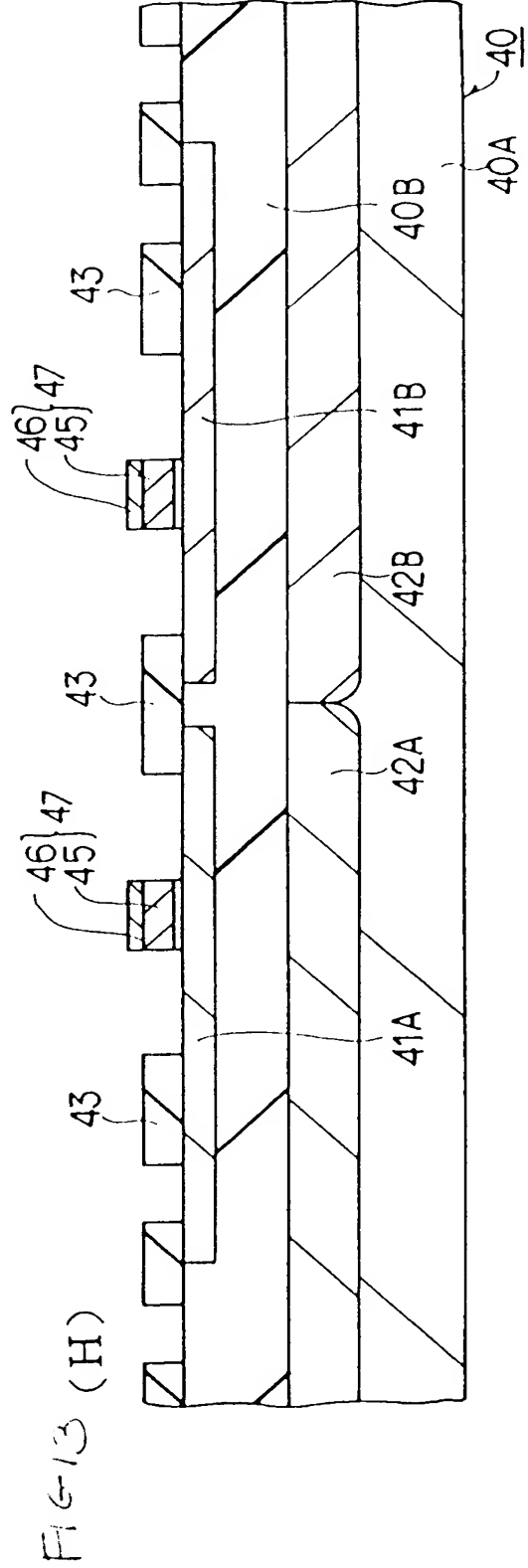
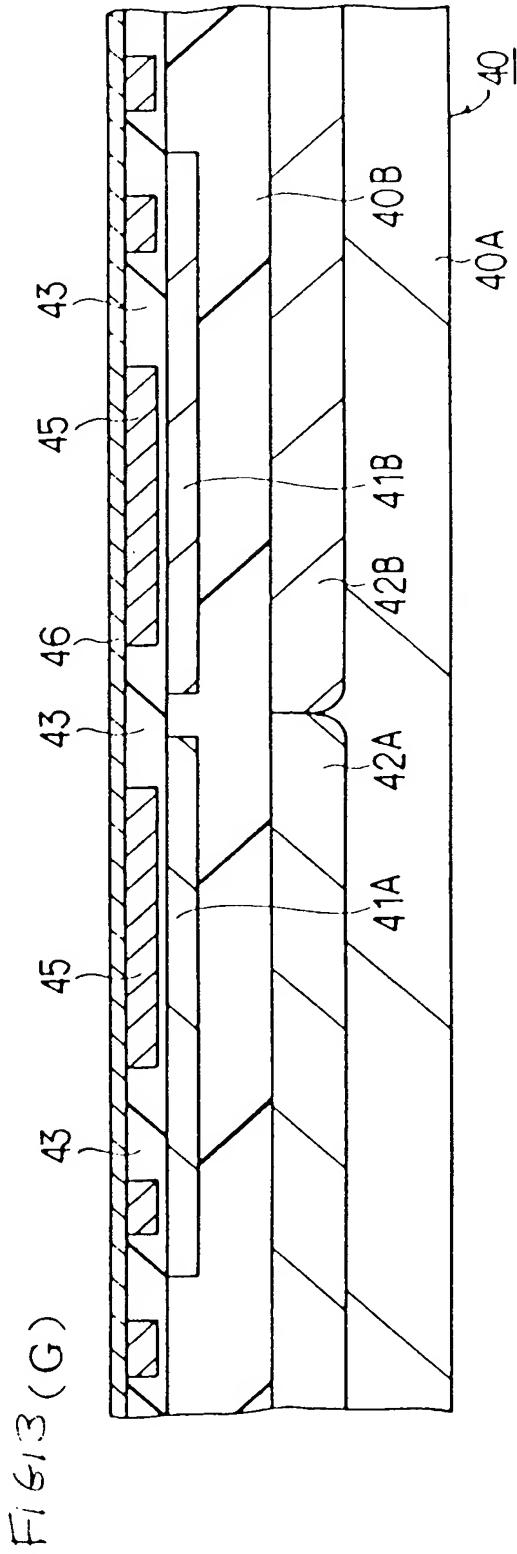


FIG. 19:-

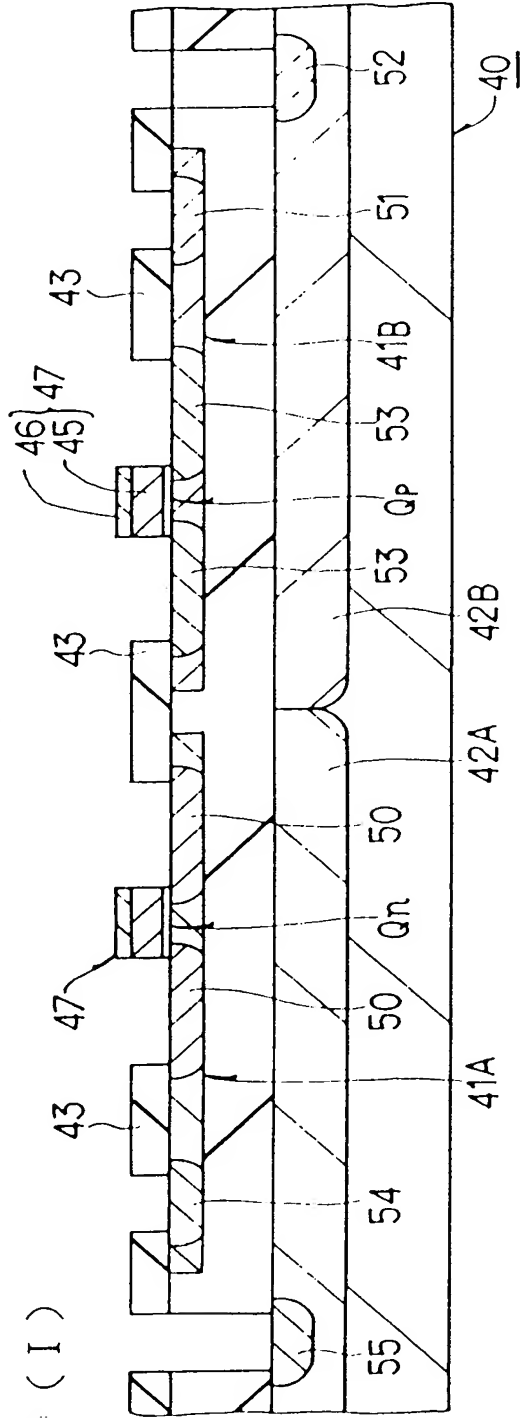
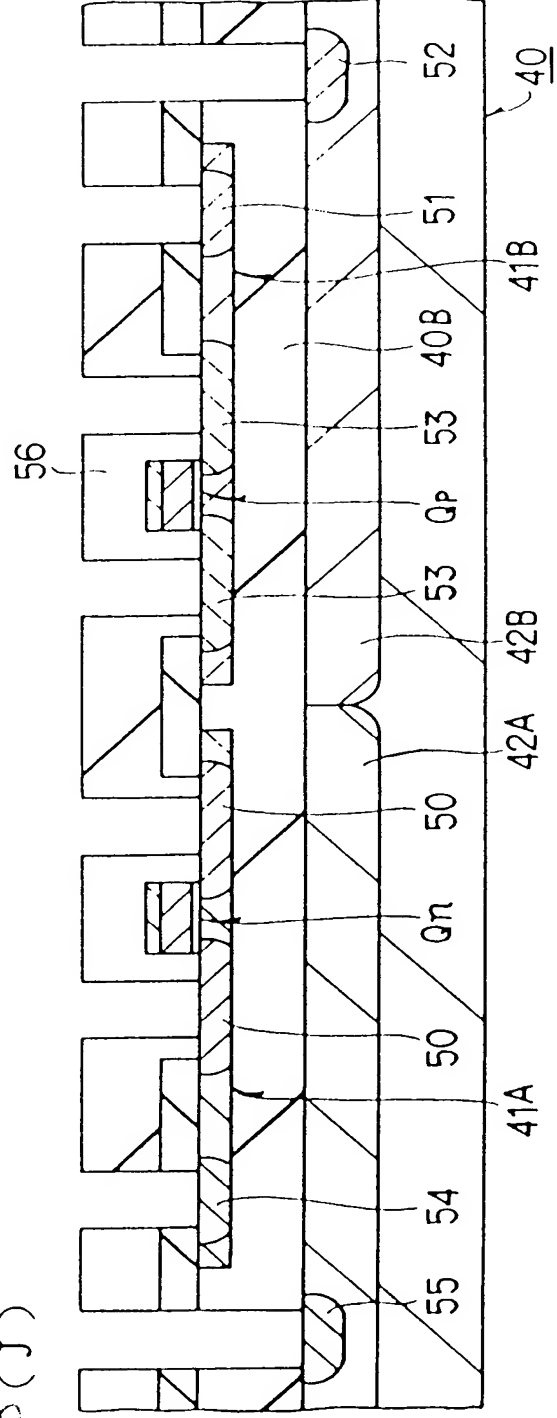


FIG. 13 (J)





1564  
FIG. 21

## (1) NORMAL OPERATION MODE

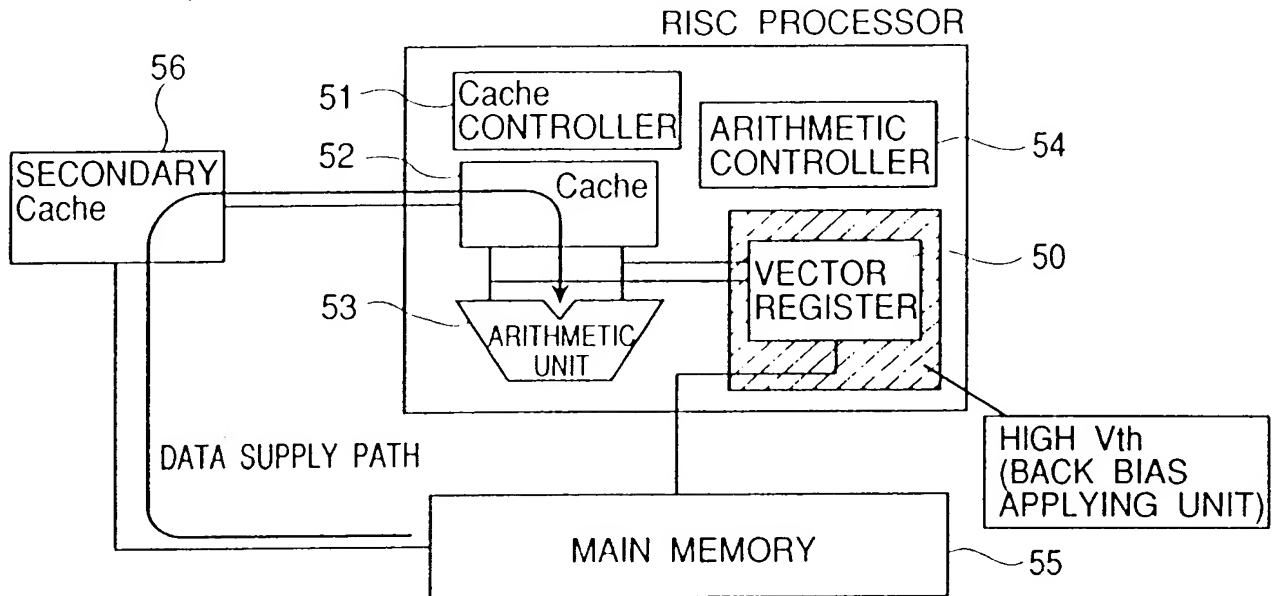


FIG 15(B)

## (2) MASS DATA NUMERICAL CALCULATION MODE (VECTOR COMPUTE MODE)

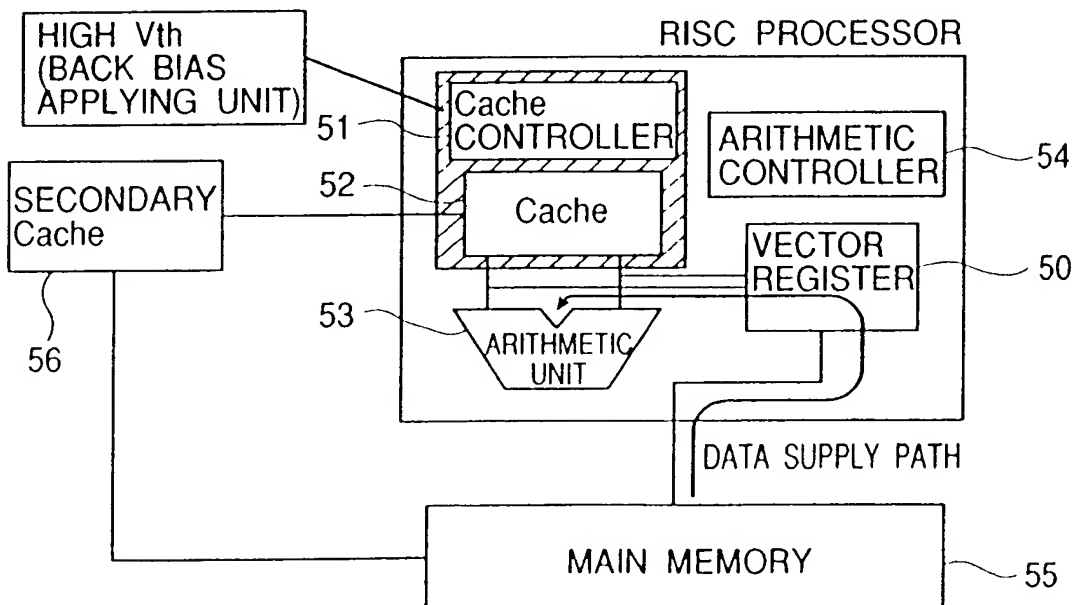


FIG. 22

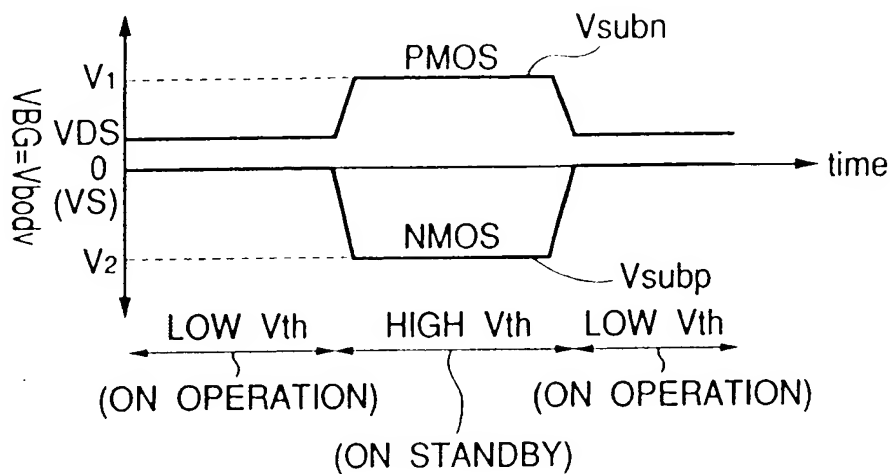


FIG. 23

